Amendments To The Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method for fabricating a sensor array having a plurality of pixels, each pixel including an electronic processing circuit having a sensor input for coupling a sensor element to the electronic processing circuit, the sensor array further having a plurality of terminal nodes for external connection to respective electronic processing circuits of multiple pixels of power, I/O and control connections, the method comprising:

integrating the electronic processing circuits on a first surface of a wafer so as to form an integrated circuit having at least one array of said electronic processing circuits with the sensor inputs and the terminal nodes ~~being accessible from a~~ on the first surface of the wafer;

in respect of each pixel, providing an electrically conductive via through the wafer extending from the respective sensor input to a second surface of the wafer opposite the first surface; and

~~depositing sensor material on the second surface of the wafer so that an unexposed surface thereof forms multiple~~

~~electrodes each in registration with a corresponding one of the electrically conductive vias~~

growing amorphous or polycrystalline sensor material on the second surface of the wafer so as to form an array of sensor elements, an unexposed surface of the sensor material forming multiple electrodes of a first polarity each in registration and in ohmic contact with a corresponding one of the electrically conductive vias and such that an exposed surface of the sensor material forms a common electrode having a polarity that is opposite to the first polarity.

2. (Currently Amended) A method for fabricating a sensor array having a plurality of pixels, each pixel including an electronic processing circuit having a sensor input for coupling a sensor element to the electronic processing circuit, the sensor array further having a plurality of terminal nodes for external connection to respective electronic processing circuits of multiple pixels of power, I/O and control connections, the method comprising:

integrating the electronic processing circuits on a first surface of a wafer so as to form an integrated circuit having at least one array of said electronic processing circuits with the sensor inputs ~~being accessible from a~~ on the first surface of the wafer;

providing a plurality of electrically conductive vias through the wafer extending to a second surface of the wafer opposite the first surface, each of said electrically conductive vias being in registration with a respective terminal node in the sensor array; and

~~depositing sensor material on the first surface of the wafer so that an unexposed surface thereof forms multiple electrodes each in registration with the respective sensor input of a corresponding electronic processing circuit~~

growing amorphous or polycrystalline sensor material on the second surface of the wafer so as to form an array of sensor elements, an unexposed surface of the sensor material forming multiple electrodes of a first polarity each in registration and in ohmic contact with a corresponding one of the electrically conductive vias and such that an exposed surface of the sensor material forms a common electrode having a polarity that is opposite to the first polarity.

3. (Previously Presented) The method according to claim 1, further including:

forming on the second surface of the wafer a plurality of metallized terminal pads each in ohmic contact with a respective one of the terminal nodes.

4. (Previously Presented) The method according to claim 1, wherein the integrated circuit includes multiple arrays of pixels and there is further included:

dividing the integrated circuit into discrete sensor arrays.

5. (Previously Presented) The method according to claim 1, further including:

assembling multiple sensor arrays edge to edge so as to form a composite sensor array having an extended surface area.

6. (Previously Presented) The method according to claim 1, further including:

thinning down the wafer from a reverse side thereof so as to remove the bulk of the wafer.

7. (Previously Presented) The method according to claim 1, wherein the wafer is pre-thinned prior to providing the electrically conductive vias through the wafer.

8. (Previously Presented) The method according to claim 1, wherein providing electrically conductive vias through the wafer includes:

coating the first surface of the wafer with photomask apart from exposed areas where the vias are to be formed; and

implanting the wafer with a material to which the photomask is impervious, so that said material penetrates only the exposed areas and creates a local increase in the conductivity of the wafer to the second surface thereof, thus forming a matrix of conductive vias.

9. (Previously Presented) The method according to Claim 8, further including:

producing a complementary photomask that covers said area of the wafer on the second surface thereof and is in precise registration with the photomask that is disposed on the first surface thereof.

10. (Previously Presented) The method according to Claim 8, wherein the wafer is based on silicon and said material is a p-type impurity.

11. (Previously Presented) The method according to claim 1, wherein providing electrically conductive vias through the wafer includes:

providing a photomask on the second surface only of the wafer so as to expose the wafer in direct registration with areas on the first surface of the wafer where the vias are to be formed;

partially etching holes through the wafer from the second surface toward the first surface so as to form partial bores; and

filling the bores with conductive material.

12. (Previously Presented) The method according to claim 1, wherein providing electrically conductive vias through the wafer includes:

partially etching holes through the wafer from the second surface so as to form partial bores;

implanting the wafer from the first surface thereof with a material to which the photomask is impervious, so that said material renders the wafer conductive directly abutting each area where vias are to be formed; and

filling the partial bores with conductive material which abuts the wafer and completes the ohmic contact to the second surface of the wafer.

13. (Previously Presented) The method according to claim 1, wherein the electrically conductive vias are formed in the wafer prior to formation of the processing circuits by:

coating the first surface of the wafer with photomask for protecting an area surrounding an intended location of each via, whilst leaving said area exposed; and

implanting the wafer with a material to which the photomask is impervious, so that said material penetrates only

said area and creates a local increase in the conductivity of the wafer from the intended location of each via to the second surface thereof, thus forming a matrix of conductive vias through the wafer.

14. (Previously Presented) The method according to claim 1, wherein the electrically conductive vias are formed in the wafer prior to formation of the processing circuits by:

coating the first surface of the wafer with photomask for protecting an area surrounding an intended location of each via, whilst leaving said area exposed, and

implanting the wafer with a material to which the photomask is impervious, so that said material penetrates only said area and creates a local increase in the conductivity of the wafer from the intended location of each via through the wafer to the second surface thereof, thus forming a matrix of conductive vias through the wafer.

15. (Previously Presented) The method according to claim 1, wherein the electrically conductive vias are formed in the wafer prior to formation of the processing circuits by:

providing a photomask on the second surface only of the wafer so as to expose the wafer in direct registration with respective locations on the first surface of the wafer of intended vias,

etching holes through the wafer from the second surface to said locations, whilst not etching all the way through the wafer so as to form bores; and

filling the bores with conductive material.

16. (Previously Presented) The method according to claim 1, wherein the electrically conductive vias are formed in the wafer prior to formation of the processing electronics by:

partially etching holes through the wafer from the second surface so as to form partial bores;

implanting the wafer from the first surface thereof with a material to which the photomask is impervious, so that said material penetrates only the intended via and renders the wafer conductive at an exposed area thereof; and

filling the partial bores with conductive material which abuts the wafer and completes the ohmic contact to the second surface of the wafer.

Claims 17-18 (Cancelled).

19. (Previously Presented) The method according to claim 13, wherein the sensor material and the terminal connections are formed on the wafer prior to formation of the processing circuits.

20. (Previously Presented) The method according to claim 1, wherein the integrated circuit includes multiple arrays

of electronic processing circuits separated by scribe lines and there is further included:

scribing along the scribe lines so as to produce individual sensor chips.

21. (Previously Presented) The method according to claim 1, further including:

connecting terminal pads metallized on an outer surface of the wafer via bump-bonds to a ceramic board that feeds bump-connections through to surface mounted pins or bores; and

encapsulating so as to form a module.

22. (Previously Presented) The method according to Claim 21, further including:

mounting several of said modules edge to edge so as to form a two-dimensional sensor of larger surface area than a single module.

23. (Currently Amended) The method according to claim 1, when used to fabricate a sensor array or module for a high energy photon imaging detector.

24. (Currently Amended) A sensor array or module manufactured according to the method of claim 1.

25. (Currently Amended) A multi-pixel sensor array comprising:

a wafer having integrated therein on a first surface of the wafer multiple electronic processing circuits each in respect of a respective pixel so as to form an integrated circuit having at least one array of electronic processing circuits each electronic processing circuit having a respective sensor input on the first surface of the wafer, the sensor array further having a plurality of terminal nodes ~~accessible from a~~ on the first surface of the wafer for external connection to respective electronic processing circuits of multiple pixels of power, I/O and control connections,

in respect of each pixel, an electrically conductive via through the wafer extending from the respective sensor input to a second surface of the wafer opposite the first surface, and

a layer of amorphous or polycrystalline sensor material ~~deposited~~ grown on the second surface of the wafer so as to form an array of sensor elements, so that an unexposed surface of the sensor material ~~thereof~~ forms multiple electrodes each in registration and in ohmic contact with a corresponding one of the electrically conductive vias, and an exposed surface of the sensor material forms a common electrode having a polarity that is opposite to the first polarity.

26. (Currently amended) A multi-pixel sensor array comprising:

a wafer having integrated therein on a first surface of the wafer multiple electronic processing circuits each in respect of a respective pixel so as to form an integrated circuit having at least one array of electronic processing circuits each electronic processing circuit having a respective sensor input ~~accessible from~~ on a first surface of the wafer, the sensor array further having a plurality of terminal nodes for external connection to respective electronic processing circuits of multiple pixels of power, I/O and control connections,

in respect of each terminal node, an electrically conductive via through the wafer extending from the respective terminal node in the sensor array to a second surface of the wafer opposite the first surface, and

a layer of sensor amorphous or polycrystalline material ~~deposited~~ grown on the first surface of the wafer so as to form an array of sensor elements, so that an unexposed surface of the sensor material ~~thereof~~ forms multiple electrodes each in registration and ohmic contact with the respective sensor input of a corresponding electronic processing circuit, and an exposed surface of the sensor material forms a common

electrode having a polarity that is opposite to the first polarity.

27. (Previously Presented) The sensor array according to Claim 25, being configured for use in a high energy photon imaging detector.

Claim 28 (Cancelled).

29. (Previously Presented) A sensor module comprising an encapsulated sensor array according to claim 25 including:

terminal pads metallized on an outer surface of the wafer via bump-bonds to a ceramic board that feeds bump-connections through to surface mounted pins or bores.

30. (Currently Amended) A multi-module sensor assembly comprising a plurality of the sensor modules according to Claim 29 mounted edge to edge so as to form a two-dimensional sensor of larger surface area than a single module.

Claim 31 (Cancelled).

32. (Previously Presented) The method according to claim 2, further including:

forming on the second surface of the wafer a plurality of metallized terminal pads each in ohmic contact with a respective one of the terminal nodes.

33. (Previously Presented) The method according to claim 2, wherein the integrated circuit includes multiple arrays of pixels and there is further included:

dividing the integrated circuit into discrete sensor arrays.

34. (Previously Presented) The method according to claim 2, further including:

assembling multiple sensor arrays edge to edge so as to form a composite sensor array having an extended surface area.

35. (Previously Presented) The method according to claim 2, further including:

thinning down the wafer from a reverse side thereof so as to remove the bulk of the wafer.

36. (Previously Presented) The method according to claim 2, wherein the wafer is pre-thinned prior to providing the electrically conductive vias through the wafer.

37. (Previously Presented) The method according to claim 2, wherein providing electrically conductive vias through the wafer includes:

coating the first surface of the wafer with photomask apart from exposed areas where the vias are to be formed; and

implanting the wafer with a material to which the photomask is impervious, so that said material penetrates only the exposed areas and creates a local increase in the conductivity of the wafer to the second surface thereof, thus forming a matrix of conductive vias.

38. (Previously Presented) The method according to Claim 37, further including:

producing a complementary photomask that covers said area of the wafer on the second surface thereof and is in precise registration with the photomask that is disposed on the first surface thereof.

39. (Previously Presented) The method according to Claim 37, wherein the wafer is based on silicon and said material is a p-type impurity.

40. (Previously Presented) The method according to claim 2, wherein providing electrically conductive vias through the wafer includes:

providing a photomask on the second surface only of the wafer so as to expose the wafer in direct registration with areas on the first surface of the wafer where the vias are to be formed;

partially etching holes through the wafer from the second surface toward the first surface so as to form partial bores; and

filling the bores with conductive material.

41. (Previously Presented) The method according to claim 2, wherein providing electrically conductive vias through the wafer includes:

partially etching holes through the wafer from the second surface so as to form partial bores;

implanting the wafer from the first surface thereof with a material to which the photomask is impervious, so that said material renders the wafer conductive directly abutting each area where vias are to be formed; and

filling the partial bores with conductive material which abuts the wafer and completes the ohmic contact to the second surface of the wafer.

42. (Previously Presented) The method according to claim 2, wherein the electrically conductive vias are formed in the wafer prior to formation of the processing circuits by:

coating the first surface of the wafer with photomask for protecting an area surrounding an intended location of each via, whilst leaving said area exposed; and

implanting the wafer with a material to which the photomask is impervious, so that said material penetrates only said area and creates a local increase in the conductivity of the wafer from the intended location of each via to the second surface thereof, thus forming a matrix of conductive vias through the wafer.

43. (Previously Presented) The method according to claim 2, wherein the electrically conductive vias are formed in the wafer prior to formation of the processing circuits by:

coating the first surface of the wafer with photomask for protecting an area surrounding an intended location of each via, whilst leaving said area exposed, and

implanting the wafer with a material to which the photomask is impervious, so that said material penetrates only said area and creates a local increase in the conductivity of the wafer from the intended location of each via through the wafer to the second surface thereof, thus forming a matrix of conductive vias through the wafer.

44. (Previously Presented) The method according to claim 2, wherein the electrically conductive vias are formed in the wafer prior to formation of the processing circuits by:

providing a photomask on the second surface only of the wafer so as to expose the wafer in direct registration with

respective locations on the first surface of the wafer of intended vias,

etching holes through the wafer from the second surface to said locations, whilst not etching all the way through the wafer so as to form bores; and

filling the bores with conductive material.

45. (Previously Presented) The method according to claim 2, wherein the electrically conductive vias are formed in the wafer prior to formation of the processing electronics by:

partially etching holes through the wafer from the second surface so as to form partial bores;

implanting the wafer from the first surface thereof with a material to which the photomask is impervious, so that said material penetrates only the intended via and renders the wafer conductive at an exposed area thereof; and

filling the partial bores with conductive material which abuts the wafer and completes the ohmic contact to the second surface of the wafer.

Claim 46 (Cancelled).

47. (Previously Presented) The method according to claim 42, wherein the sensor material and the terminal connections are formed on the wafer prior to formation of the processing circuits.

48. (Previously Presented) The method according to claim 2, wherein the integrated circuit includes multiple arrays of electronic processing circuits separated by scribe lines and there is further included:

scribing along the scribe lines so as to produce individual sensor chips.

49. (Previously Presented) The method according to claim 2, further including:

connecting terminal pads metallized on an outer surface of the wafer via bump-bonds to a ceramic board that feeds bump-connections through to surface mounted pins or bores; and

encapsulating so as to form a module.

50. (Previously Presented) The method according to Claim 49, further including:

mounting several of said modules edge to edge so as to form a two-dimensional sensor of larger surface area than a single module.

51. (Currently Amended) The method according to claim 2, when used to fabricate a sensor array or module for a high energy photon imaging detector.

52. (Currently Amended) A sensor array or module manufactured according to the method of claim 2.